KiCad

KiCad will not kick your ass

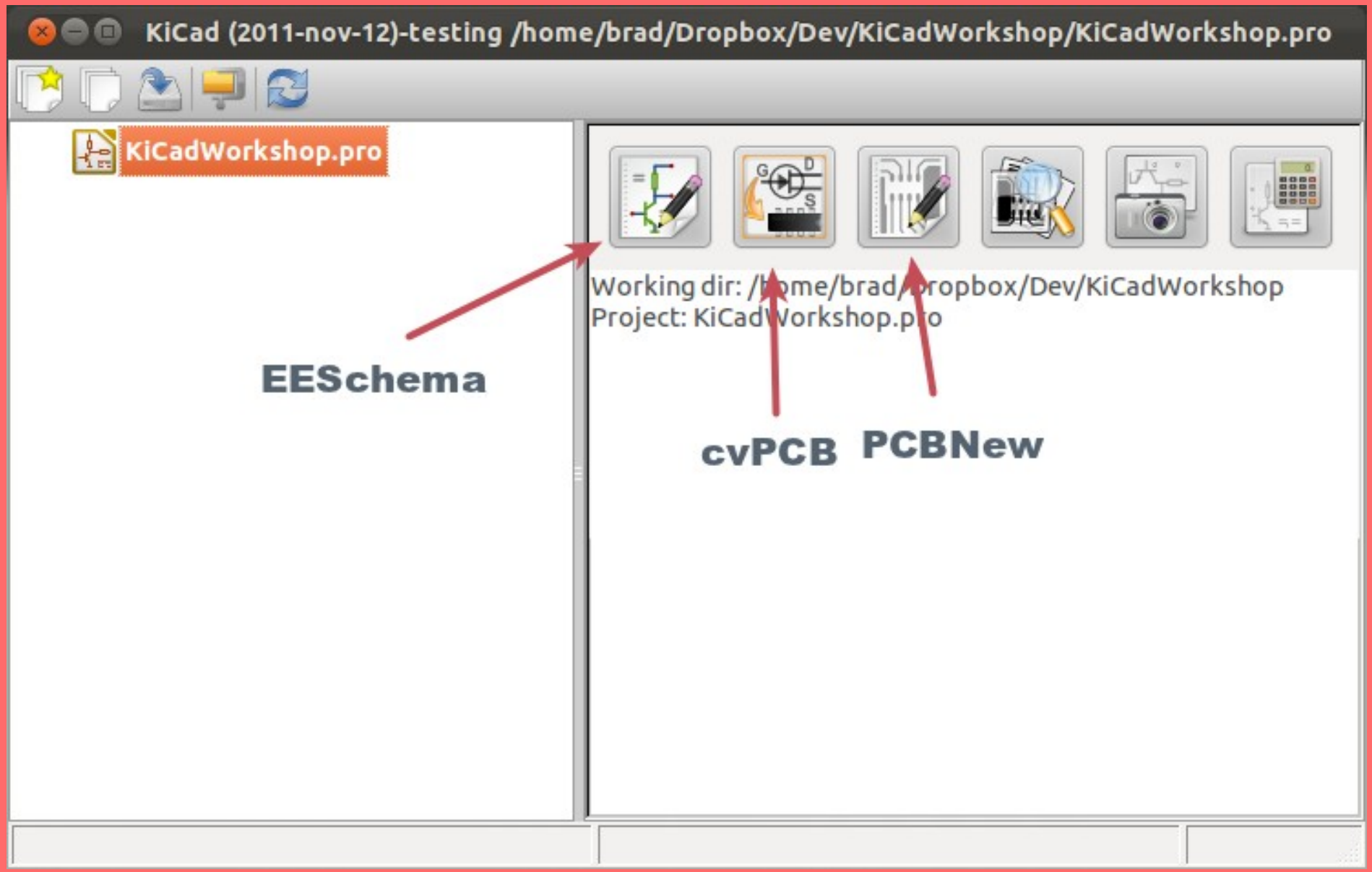
(and you will eventually like it)

Free

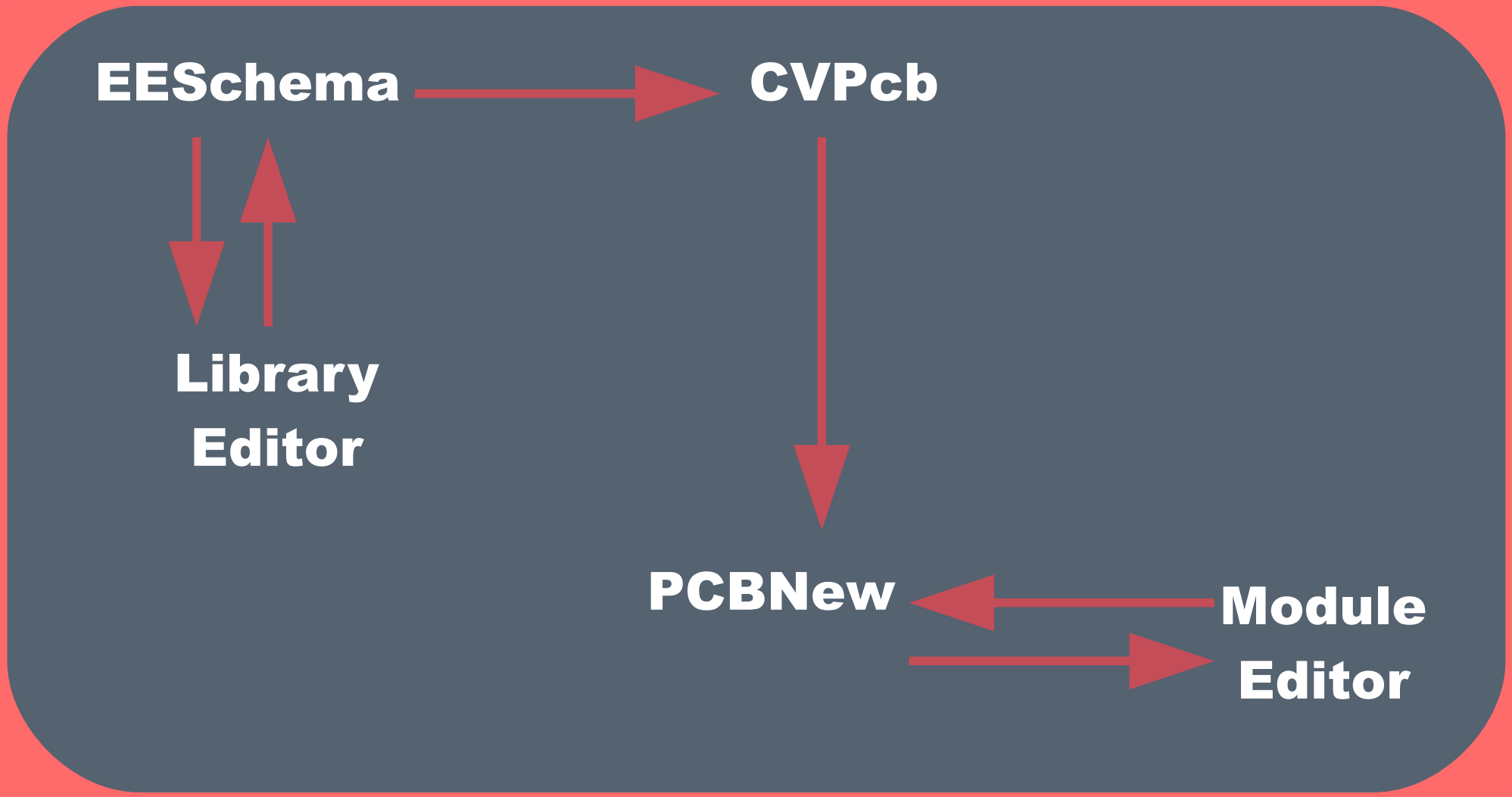
THE BULLET POINTS

- CROSS PLATFORM
- TEXT-BASED FILE FORMAT
- UNLIMITED (THAT'S RIGHT, UNLIMITED)
  - BOARD SIZE
  - BOARD LAYERS
- HIERARCHICAL SHEETS

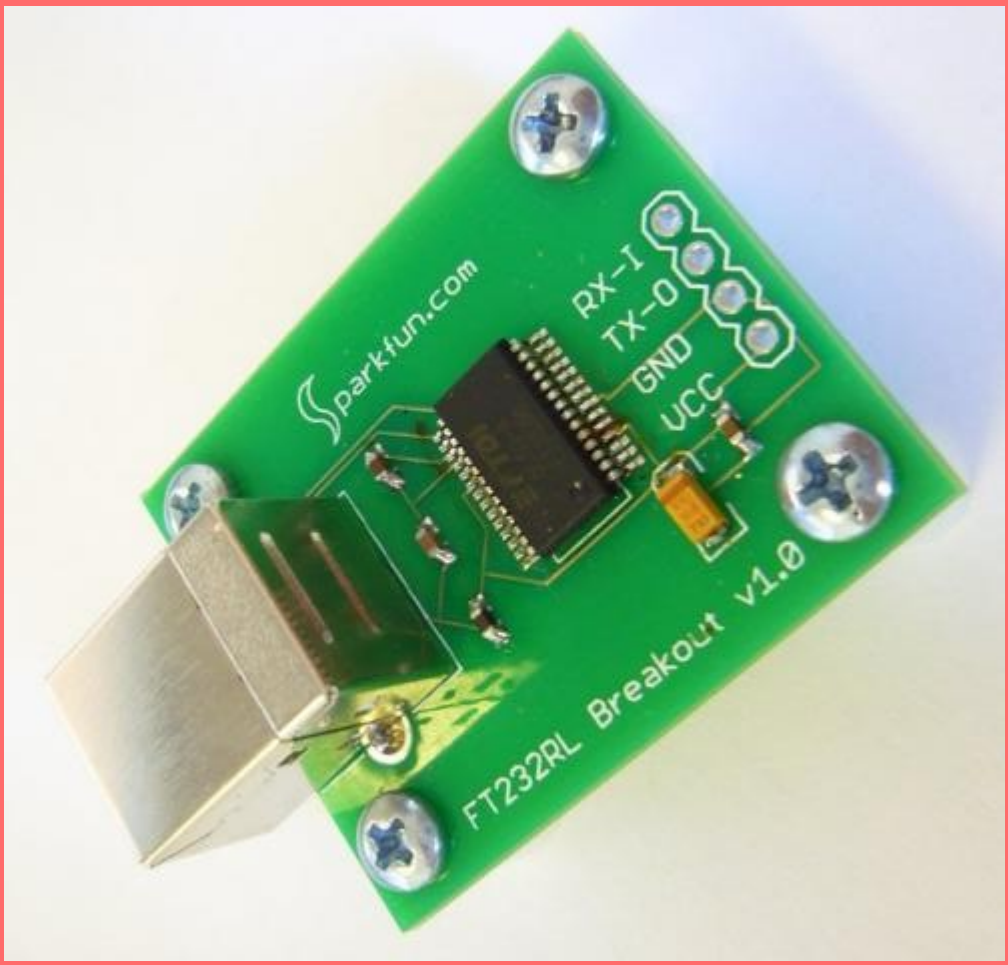
How to KiCad


KiCad (2011-nov-12)-testing /home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.pro
KiCadWorkshop.pro
Working dir: /home/brad/Dropbox/Dev/KiCadWorkshop
Project: KiCadWorkshop.pro
EESchema
cvPCB
PCBNew

Design Flow



FTDI Serial Adapter Thing



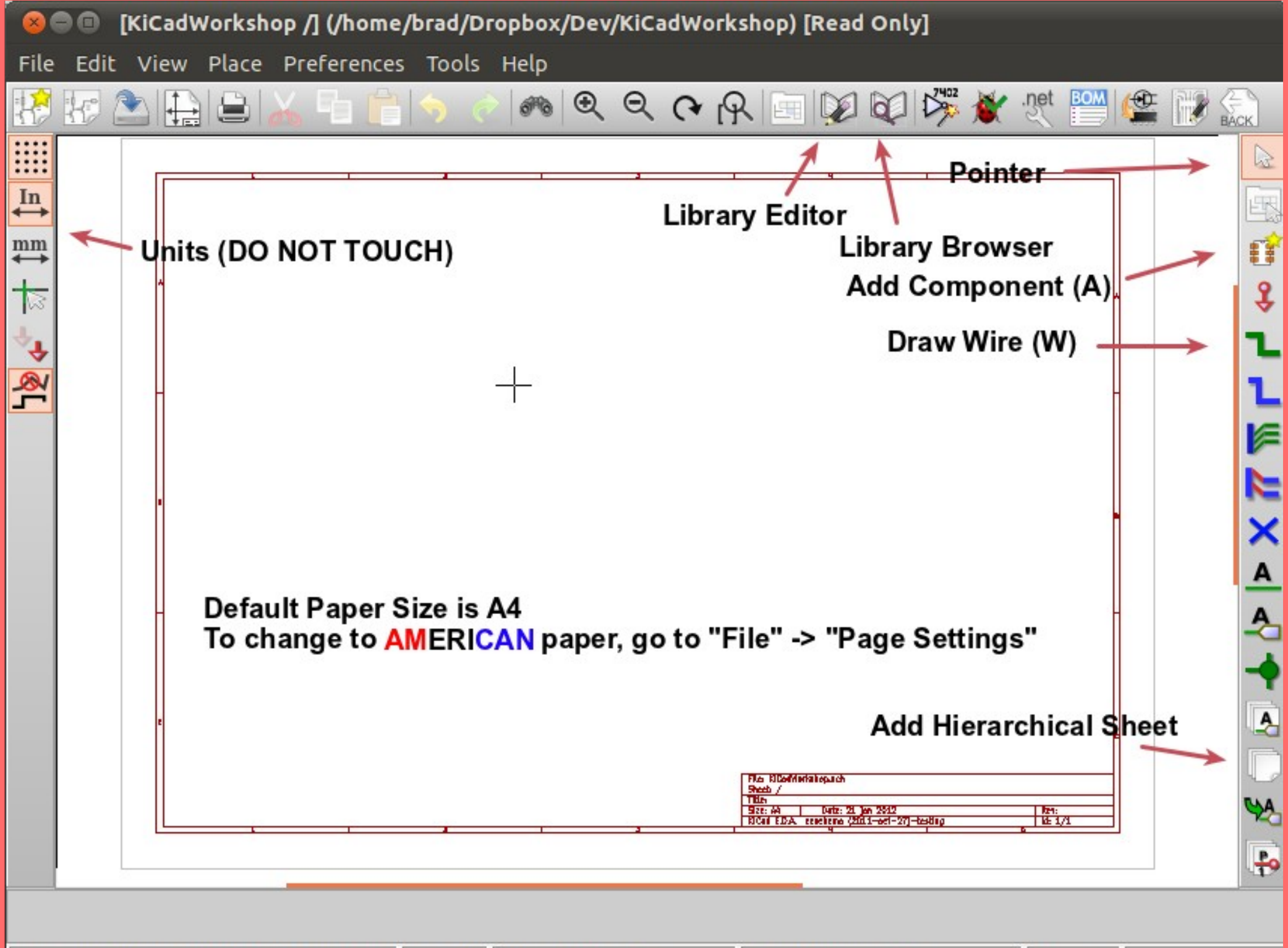
EESchema

EESchema: Keyboard Shortcuts of Great Import

- A: Add
- M: Move
- R: Rotate
- W: Wire
- E: Edit
- V: Value
- ?: List Keyboard Shortcuts

Schematic Capture Flow

1. Place all components
2. Wire components together
3. Label nets
4. Annotate Schematic
5. Generate Netlist

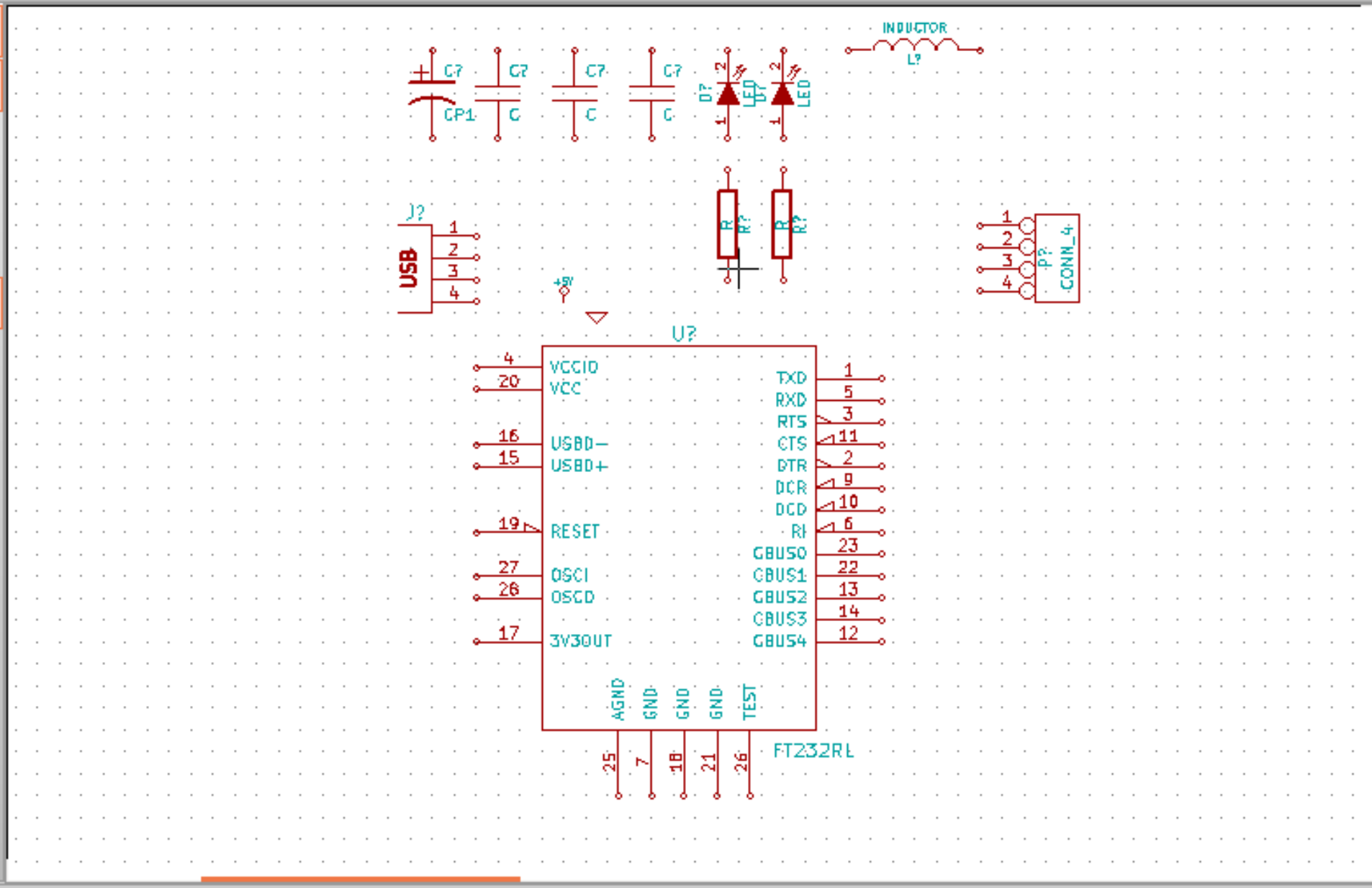

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]
File Edit View Place Preferences Tools Help
Pointer
Library Editor
Library Browser
Units (DO NOT TOUCH)
Add Component (A)
Draw Wire (W)
Default Paper Size is A4
To change to AMERICAN paper, go to "File" -> "Page Settings"
Add Hierarchical Sheet
Library /usr/share/kicad/library/valve:
Z 17.045
X 4.450 Y 2.800
dx 4.450 dy 2.800
Inches

Parts needed for FTDI Serial Adapter Thing!

- 3x “C” (Capacitor)
- 1x “CP1” (Capacitor, Polarized)
- 1x “Inductor”
- 1x “USB_2”
- 1x “CONN_4”
- 2x “LED”
- 2x “R” (Resistor)
- 1x “FT232RL”
- +5V, GND

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]

File Edit View Place Preferences Tools Help



Reference	Name	Component	Library	Description	Key words
J?	USB_2	USB_2	conn	USB Connector	USB usb CONNECTOR connector

File /home/brad/Dropbox/Dev/KiCad\ | Z 8 | X 3.950 Y 3.950 | dx 3.950 dy 3.950 | Inches

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]

File Edit View Place Preferences Tools Help

Move Component J? M
Drag Component G
Orient Component
Edit Component
Copy Component C
Delete Component Delete
Center F4
Zoom in F1
Zoom out F2
Redraw view F3
Zoom auto Home
Zoom select
Grid Select
Close

Edit E
Value V
Reference
Footprint F
Edit with Library Editor

Reference	Name	Component	Library	Description	Key words
J?	USB_2	USB_2	conn	USB Connector	USB usb CONNECTOR connector

File /home/brad/Dropbox/Dev/KiCad\ | Z 8 | X 2.600 Y 3.900 | dx 2.600 dy 3.900 | Inches

Component Library Editor: /usr/share/kicad/library/conn.lib [Read Only]

File Edit View Place Preferences Help

J?

USB

1 VCC

2 D+

3 D-

4 G

USB_2

Type	Unit	Convert	Name	Number	Type	Style
Pin	1	no	~	1	Input	Line

Z 2 X 0.050 Y -0.150

Pin Properties

Pin name: VCC

Pin number: 1

Orientation: Left

Electrical type: Input

Graphic Style: Line

Name text size: 0.050 inches

Number text size: 0.050 inches

Length: 0.200 inches

Sharing

- [ ] Shared by all parts in component
- [ ] Shared by all body styles (DeMorgan)

Schematic Properties

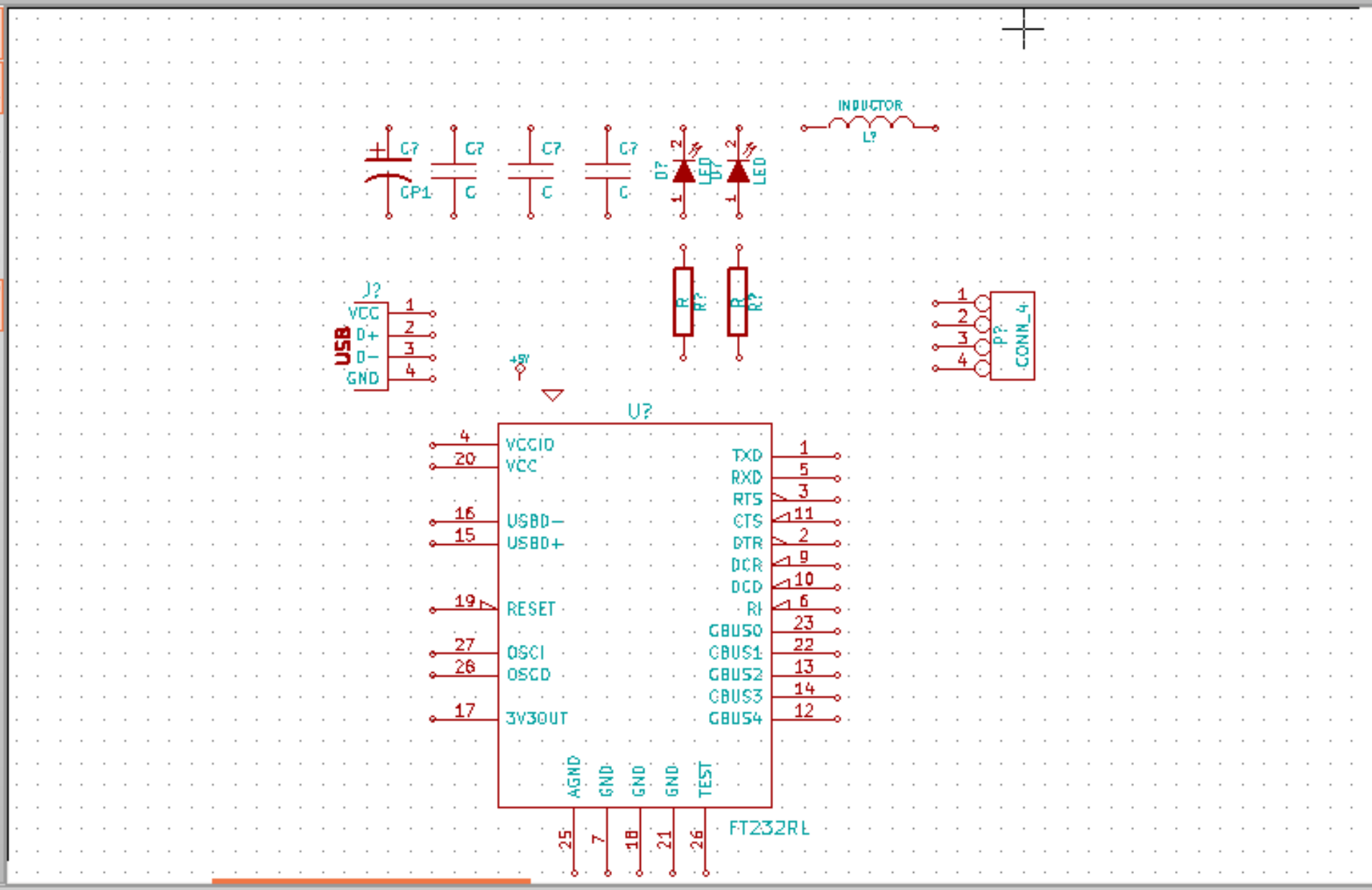
- [x] Visible

VCC 1

Cancel OK

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]

File Edit View Place Preferences Tools Help

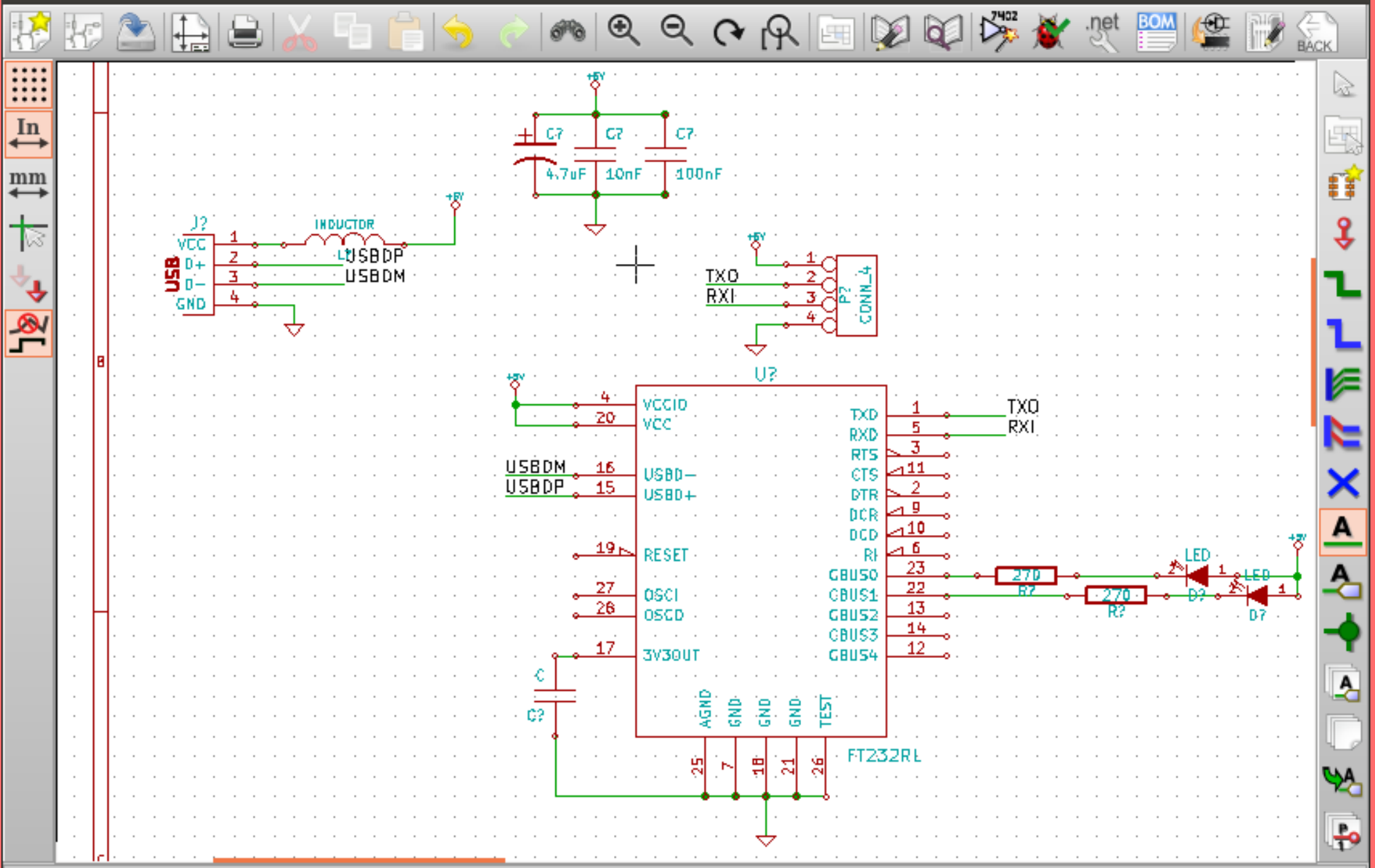


Reference	Name	Component	Library	Description	Key words
J?	USB_2	USB_2	conn	USB Connector	USB usb CONNECTOR connector

File /home/brad/Dropbox/Dev/KiCad | Z 8 | X 5.500 Y 2.450 | dx 5.500 dy 2.450 | Inches

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]

File Edit View Place Preferences Tools Help



Reference	Power symbol	Component	Library	Description	Key words
#PWR?	GND	GND	power		

File /home/brad/Dropbox/Dev/KiCad\ | Z 8 | X 5.350 Y 3.950 | dx 3.950 dy 3.350 | Inches | Add label

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]

File Edit View Place Preferences Tools Help

Annotate Schematic

Scope

- (•) Use the entire schematic
- ( ) Use the current page only

- (•) Keep existing annotation
- ( ) Reset existing annotation

Annotation Order

- (•) Sort components by X position
- ( ) Sort components by Y position

Annotation Choice

- (•) Use first free number in schematic
- ( ) Start to sheet number*100 and use first free number
- ( ) Start to sheet number*1000 and use first free number

Close | Clear Annotation | Annotation

Reference	Power symbol	Component	Library	Description	Key words
#PWR?	GND	GND	power		

File /home/brad/Dropbox/Dev/KiCad\ | Z 8 | X 5.050 Y 2.650 | dx 5.050 dy 2.650 | Inches | Add label

[KiCadWorkshop /] (/home/brad/Dropbox/Dev/KiCadWorkshop) [Read Only]

File Edit View Place Preferences Tools Help

Netlist

Pcbnew | OrcadPCB2 | CadStar | Spice | Add Plugin

Options:

Default format

Netlist

Cancel

Reference #PWR? | Power symbol GND | Component GND | Library power | Description | Key words

File /home/brad/Dropbox/Dev/KiCad\ | Z 8 | X 5.100 Y 2.650 | dx 5.100 dy 2.650 | Inches | Add label

Done with EESchema!

Done with EESchema!

CVPCB

CVPCB Flow

1. Hope the default footprints work for your parts
2. #!$@%, they don't
3. Assign as many footprints as you can
4. Go into PCBNew, create new modules
5. Goto 1

REMIND THEM THAT CVPCB MAPS PINS BY NUMBER AND ALSO THAT PIN NUMBERS DON'T HAVE TO BE NUMBERS, THEY CAN CONTAIN ANY ASCII CHARACTER

CvPcb (2011-oct-27)-testing /home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.net

File Preferences Help

1	C1 -	4.7uF	:
2	C2 -	C	:
3	C3 -	10nF	:
4	C4 -	100nF	:
5	D1 -	LED	:
6	D2 -	LED	:
7	J1 -	USB_2	:
8	L1 -	INDUCTOR	:
9	P1 -	CONN_4	:
10	R1 -	270	:
11	R2 -	270	:
12	U1 -	FT232RL	:

Save

Show selected footprint

Filter Footprints

Don't Filter Footprints

Footprint List

1 CP4
2 CP5
3 CP6
4 CP8
5 CP10
6 CP12
7 CP14
8 CP16
9 CP18
10 CP20
11 CP36V
12 CPR10X16
13 SM0402
14 SM0603
15 SM0603_Capa
16 SM0603_Resistor
17 SM0805
18 SM1206
19 SM1206POL
20 SM1210
21 SM1210L
22 SM1812
23 SM1812E
24 SM1812L
25 SM2112L
26 SM2512
27 SMD403
28 SMDHD/VF
29 SMDSVP10

Components: 12 (free: 12)

Footprints (filtered): 29

CvPcb (2011-oct-27)-testing /home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.net

File Preferences Help

1	C1 -	4.7uF	:
2	C2 -	C	:
3	C3 -	10nF	:
4	C4 -	100nF	:
5	D1 -	LED	:
6	D2 -	LED	:
7	J1 -	USB_2	:
8	L1 -		
9	P1 -		
10	R1 -		
11	R2 -		
12	U1 -		

Footprint: CP4

CP4 C*** | Netlist path | Layer Front | Pads 2 | Stat .. | Orient 0.0 | Module CP4 | 3D-Shap discret/c

Z 9.1548 | X 0.1000 Y -0.1500 | dx 0.1000 dy -0.1500 | Inches

1	CP4
2	CP5
3	CP6
4	CP8
5	CP10
6	CP12
7	CP14
8	CP16
9	CP18
10	CP20
11	CP36V
12	CPR10X16
13	SM0402
14	SM0603
15	SM0603_Capa
16	SM0603_Resistor
17	SM0805
18	SM1206
19	SM1206POL
20	SM1210
21	SM1210L
22	SM1812
23	SM1812E
24	SM1812L
25	SM2112L
26	SM2512
27	SMD403
28	SMDHD/VF
29	SMDSVP10

Condensateur polarise | KeyW: CP | Footprints (filtered): 29

CvPcb (2011-oct-27)-testing /home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.net

File Preferences Help

1	C1	-	4.7uF	: CP4
2	C2	-	C	: C1
3	C3	-	10nF	: C1
4	C4	-	100nF	: C1
5	D1	-	LED	: LED-5MM
6	D2	-	LED	: LED-5MM
7	J1	-	USB_2	: USB_B
8	L1	-	INDUCTOR	: R3
9	P1	-	CONN_4	: SIL-4
10	R1	-	270	: R3
11	R2	-	270	: R3
12	U1	-	FT232RL	: SSOP28

1 CP4
2 CP5
3 CP6
4 CP8
5 CP10
6 CP12
7 CP14
8 CP16
9 CP18
10 CP20
11 CP36V
12 CPR10X16
13 SM0402
14 SM0603
15 SM0603_Capa
16 SM0603_Resistor
17 SM0805
18 SM1206
19 SM1206POL

Components: 12 (free: 0)

Footprints (filtered): 29

Done with CVPCB!

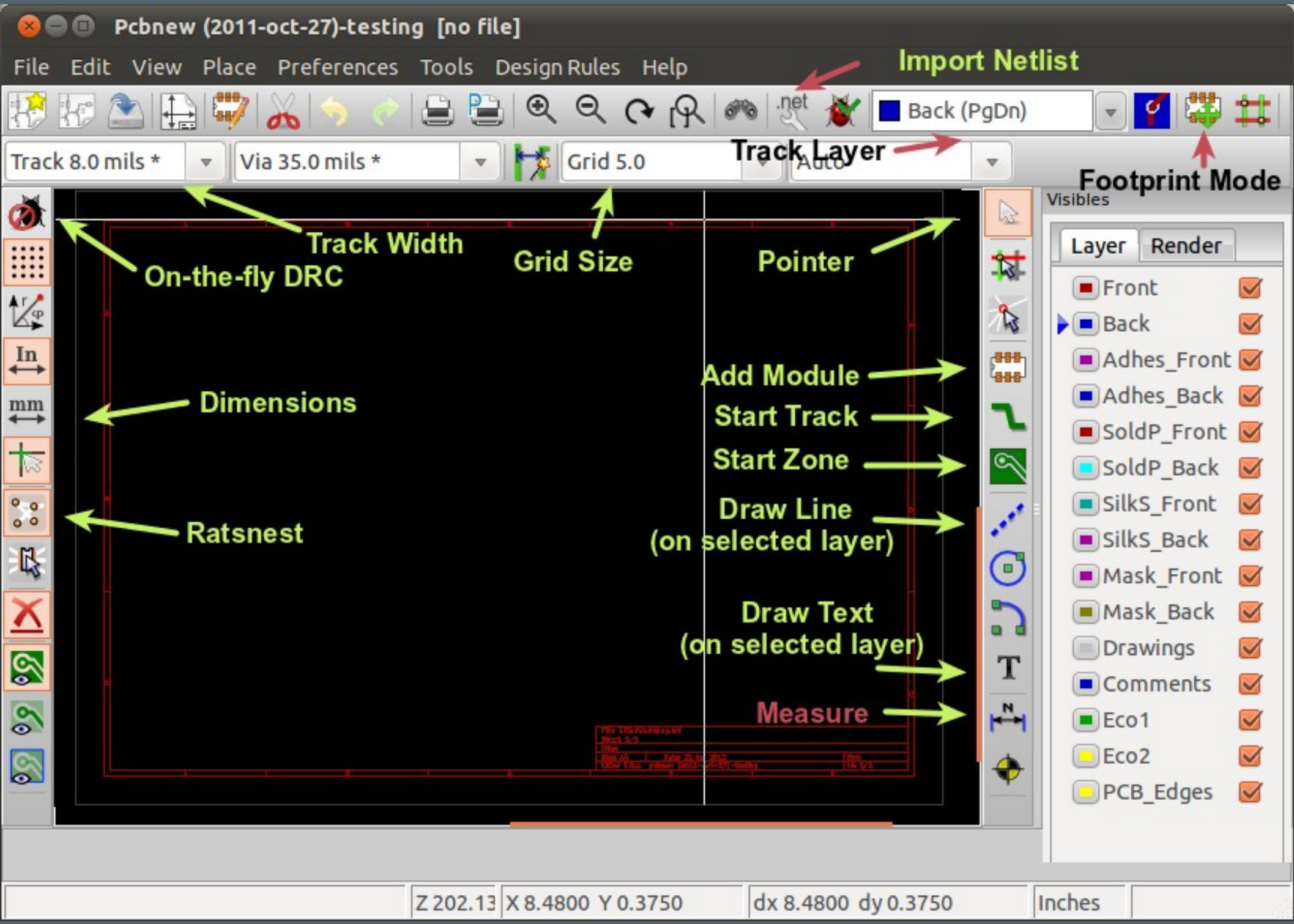
PCBNew

PCBNew Flow

1. Import Netlist
2. Define board outline
3. Define design rules
4. Explode modules
5. Show the ratsnest
6. Arrange parts to minimize ratsnest
7. Route tracks, vias, etc.
8. Draw planes
9. Generate gerbers
10. Generate drill file

Keyboard Shortcuts

- Delete Track/Footprint (Del)
- Delete track segment (Bksp)
- New track (X)
- New via (V)
- Change track direction (/)
- Drag item, keep slope (D)
- Place Item (P)
- End track (End)
- Move item (M)
- Flip item (F)
- Rotate Item (R)
- Edit Item (E)
- Next Copper Layer (PgUp)
- Prev Copper Layer (PgDn)


Pcbnew (2011-oct-27)-testing [no file]
File Edit View Place Preferences Tools Design Rules Help
Import Netlist
.net
Back (PgDn)
Track Layer
Footprint Mode
Track 8.0 mils *
Via 35.0 mils *
Grid 5.0
Auto
Track Width
On-the-fly DRC
Grid Size
Pointer
Dimensions
Ratsnest
Add Module
Start Track
Start Zone
Draw Line
(on selected layer)
Draw Text
(on selected layer)
Measure
Visibles
Layer
Render
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Z 202.13
X 8.4800 Y 0.3750
dx 8.4800 dy 0.3750
Inches

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

Track 8.0 mils *

Netlist

Module Selection:
- Reference
- Timestamp

Bad Tracks Deletion:
- Keep
- Delete

Exchange Module:
- Keep
- Change

Extra Footprints
- Keep
- Delete

Browse Netlist Files

Read Current Netlist

Footprints Test

Rebuild Board Connectivity

Close

Netlist File:

/home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.net

Messages:

Reading Netlist "/home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.net"
Using component/footprint link file "/home/brad/Dropbox/Dev/KiCadWorkshop/KiCadWorkshop.cmp"

Visibles

Layer Render

Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges

Pads 56 Vias 0 tracks 0

Z 202.13 X 8.4800 Y 0.3750 dx 8.4800 dy 0.3750 Inches

Design Rules Editor

Net Classes Editor | Global Design Rules

Net Classes:

	Clearance	Track Width	Via Dia	Via Drill	uVia Dia	uVia Drill
Default	0.0100	0.0160	0.0350	0.0250	0.0200	0.0050
Power	0.0100	0.0240	0.0350	0.0250	0.0200	0.0050

Add | Remove | Move Up

Membership:

* (Any)

Net	Class
	Default
/RXI	Default
/TXO	Default
/USBDM	Default
/USBDP	Default
N-000013	Default
N-000016	Default
N-000018	Default
N-000019	Default
N-000020	Default
N-000021	Default
+5V	Power
GND	Power

<<< | >>> | << Select All | Select All >>

Power

Net	Class
+5V	Power
GND	Power

Messages:

Current general settings:
Minimum value for tracks width: **0.0080 "**
Minimum value for vias diameter: **0.0350 "**
Minimum value for microvias diameter: **0.0200 "**

OK | Cancel

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

PCB_Edges

Track 16.0 mils * | Via 35.0 mils * | Grid 50.0 | Zoom 80

J1

Visibles

Layer Render

- Front
- Back
- Adhes_Front
- Adhes_Back
- SoldP_Front
- SoldP_Back
- SilkS_Front
- SilkS_Back
- Mask_Front
- Mask_Back
- Drawings
- Comments
- Eco1
- Eco2
- PCB_Edges

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
56	0	0	40	13	28	0	28

Z 80 | X 2.7000 Y -0.0500 | dx 2.7000 dy -0.0500 | Inches | Add graphic lin

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

Front (PgUp)

Track 16.0 mils * | Via 35.0 mils * | Grid 50.0 | Zoom 80

Footprint L1 (Front)
Lock Module L
Auto Place Module
Get and Move Footprint T
Glob Move and Place
Select Working Layer
Center F4
Zoom in F1
Zoom out F2
Redraw view F3
Zoom auto Home
Zoom select
Grid Select
Close

Unlock All Modules
Lock All Modules
Move All Modules
Move New Modules
Autoplace All Modules
Autoplace New Modules
Autoplace Next Module
Orient All Modules

Visibles

Layer | Render

Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges

L1	Last Change	Layer	Pads	Stat	Orient	Module	3D-Shape
INDUCTOR	Aug 17, 2011	Front	2	..	0.0	R3	discret/resistor.wrl

KeyW: R

Z 80 | X 0.0000 Y 0.0500 | dx 0.0000 dy 0.0500 | Inches

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

Front (PgUp)

Track 16.0 mils * | Via 35.0 mils * | Grid 50.0 | Zoom 50

Visibles

Layer Render

- Front
- Back
- Adhes_Front
- Adhes_Back
- SoldP_Front
- SoldP_Back
- SilkS_Front
- SilkS_Back
- Mask_Front
- Mask_Back
- Drawings
- Comments
- Eco1
- Eco2
- PCB_Edges

R1	Last Change	Layer	Pads	Stat	Orient	Module	3D-Shape
270	Aug 17, 2011	Front	2	..	0.0	R3	discret/resistor.wrl

KeyW: R

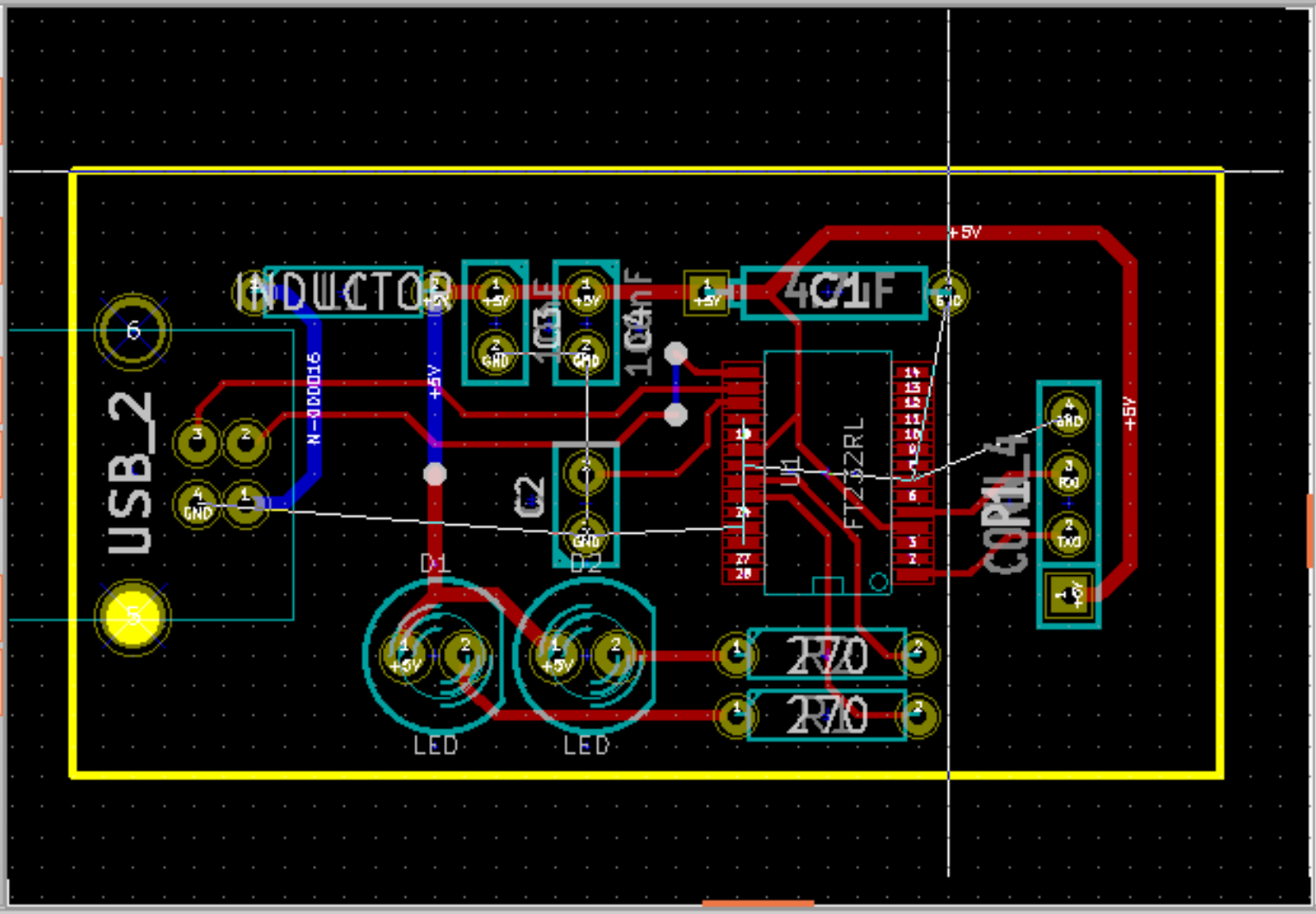
Z 50 | X 3.2500 Y 0.6500 | dx 3.2500 dy 0.6500 | Inches

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

Back (PgDn)

Track 24.0 mils * | Via 35.0 mils * | Grid 50.0 | Zoom 35



Visibles

Layer | Render

- Front
- Back
- Adhes_Front
- Adhes_Back
- SoldP_Front
- SoldP_Back
- SilkS_Front
- SilkS_Back
- Mask_Front
- Mask_Back
- Drawings
- Comments
- Eco1
- Eco2
- PCB_Edges

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
56	3	71	40	13	28	18	10

links 28 nc 10 net:nc 28 | Z 35 | X 2.3500 Y 1.0000 | dx 2.3500 dy 1.0000 | Inches | Add tracks

Zone Properties

Layer:

- Front
- Back

Net:

- <no net>
- GND
- +5V
- /RXI
- /TXO
- /USBDM
- /USBDP
- N-000013
- N-000016

Net Filtering

Display: Show all (advanced)

Hidden net filter: N-*

Visible net filter: *

Apply Filters

Settings

Clearance (''): 0.0200

Minimum width (''): 0.0100

Corner smoothing: None

Chamfer distance (mm): 0.0000

Pad connection: Thermal relief

Thermal Reliefs

Antipad clearance (''): 0.0100

Spoke width (''): 0.0200

Fill mode: Polygon

Segments / 360 deg: 16

Outline slope: Arbitrary

Outline style: Hatched

Export Settings to Other Zones | Ok | Cancel

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

Front (PgUp)

Track 10.0 mils | Via 35.0 mils * | Grid 50.0 | Auto

Visibles

Layer Render

- Front
- Back
- Adhes_Front
- Adhes_Back
- SoldP_Front
- SoldP_Back
- SilkS_Front
- SilkS_Back
- Mask_Front
- Mask_Back
- Drawings
- Comments
- Eco1
- Eco2
- PCB_Edges

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
56	3	85	40	13	28	28	0

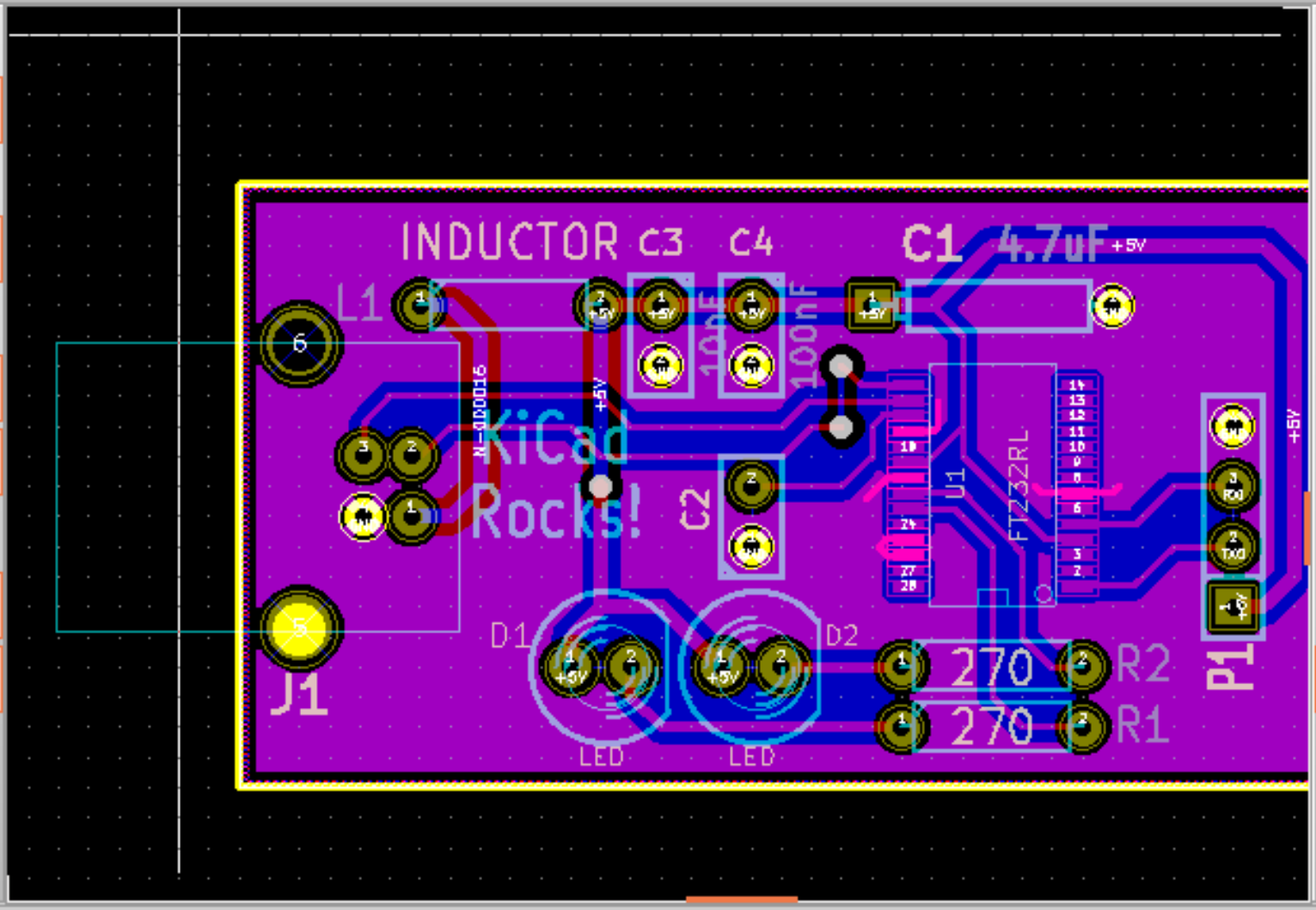
links 28 nc 0 net:nc 28 | Z 37.567 | X 2.2500 Y 0.6000 | dx 2.2500 dy 0.6000 | Inches | Add tracks

Pcbnew (2011-oct-27)-testing [no file]

File Edit View Place Preferences Tools Design Rules Help

SilkS_Front

Track 10.0 mils | Via 35.0 mils * | Grid 25.0 | Zoom 35



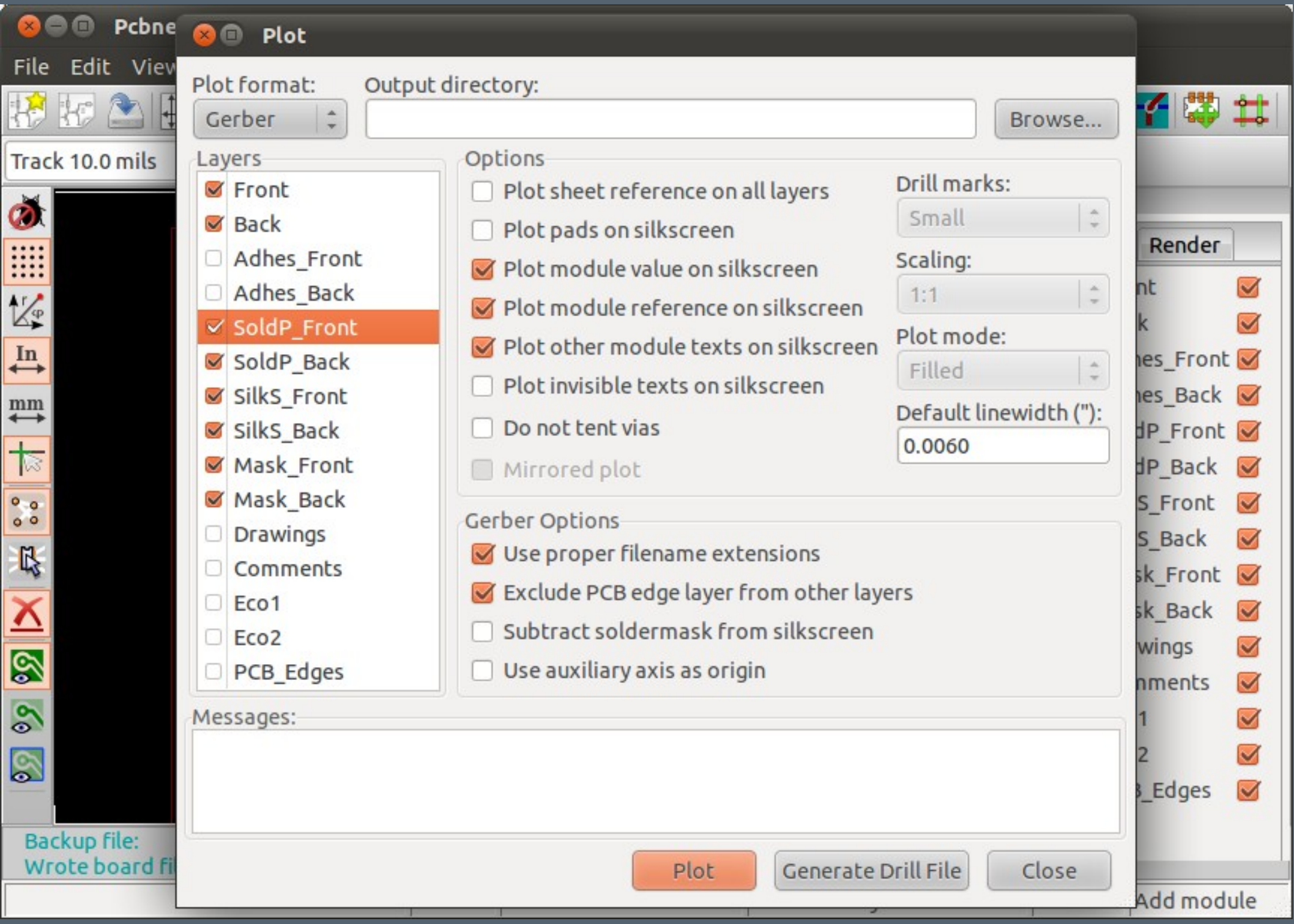
Visibles

Layer | Render

- Front
- Back
- Adhes_Front
- Adhes_Back
- SoldP_Front
- SoldP_Back
- SilkS_Front
- SilkS_Back
- Mask_Front
- Mask_Back
- Drawings
- Comments
- Eco1
- Eco2
- PCB_Edges

Pads	Vias	trackSegm	Nodes	Nets	Links	Connect	Unconnected
56	3	85	40	13	28	28	0

links 28 nc 0 net:nc 28 | Z 35 | X 0.8000 Y 0.7500 | dx 0.8000 dy 0.7500 | Inches | Add text


Pcbne
File Edit View
Track 10.0 mils
Plot
Plot format:
Gerber
Output directory:
Browse...
Layers
Front
Back
Adhes_Front
Adhes_Back
SoldP_Front
SoldP_Back
SilkS_Front
SilkS_Back
Mask_Front
Mask_Back
Drawings
Comments
Eco1
Eco2
PCB_Edges
Options
Plot sheet reference on all layers
Plot pads on silkscreen
Plot module value on silkscreen
Plot module reference on silkscreen
Plot other module texts on silkscreen
Plot invisible texts on silkscreen
Do not tent vias
Mirrored plot
Drill marks:
Small
Scaling:
1:1
Plot mode:
Filled
Default linewidth (''):
0.0060
Gerber Options
Use proper filename extensions
Exclude PCB edge layer from other layers
Subtract soldermask from silkscreen
Use auxiliary axis as origin
Messages:
Plot
Generate Drill File
Close
Render
Backup file:
Wrote board fi
Add module

Pcbne

File Edit View

Track 10.0 mils

Plot

Plot format: Output directory:

Drill Files Generation

Drill Units:
- Millimeters
- Inches

Zeros Format
- Decimal format
- Suppress leading zeros
- Suppress trailing zeros
- Keep zeros

Precision
- 2:3
- 2:4

Drill Origin:
- Absolute
- Auxiliary axis

Drill Sheet:
- None
- Drill map (HPGL)
- Drill map (PostScript)
- Drill map (Gerber)
- Drill map (DXF)

Drill Report:
- None
- Drill report

HPGL plotter Options:

Speed (cm/s): 20

Pen Number: 1

Options:
- Mirror y axis
- Minimal header

Info:

Default Vias Drill: Use Netclasses values

Micro Vias Drill: Use Netclasses values

Holes Count:
- Plated Pads: 27
- Not Plated Pads: 1
- Through Vias: 3
- Micro Vias: 0
- Buried Vias: 0

OK

Cancel

Plot | Generate Drill File | Close

Render

nt
k
nes_Front
nes_Back
dP_Front
dP_Back
S_Front
S_Back
sk_Front
sk_Back
wings
nments
1
2
_Edges

Backup file:
Wrote board fi

Add module

Module Editor (no active library)

File Edit View Place Help

Grid 20.0 | Auto

Dimensions

Add Pad

Add Line

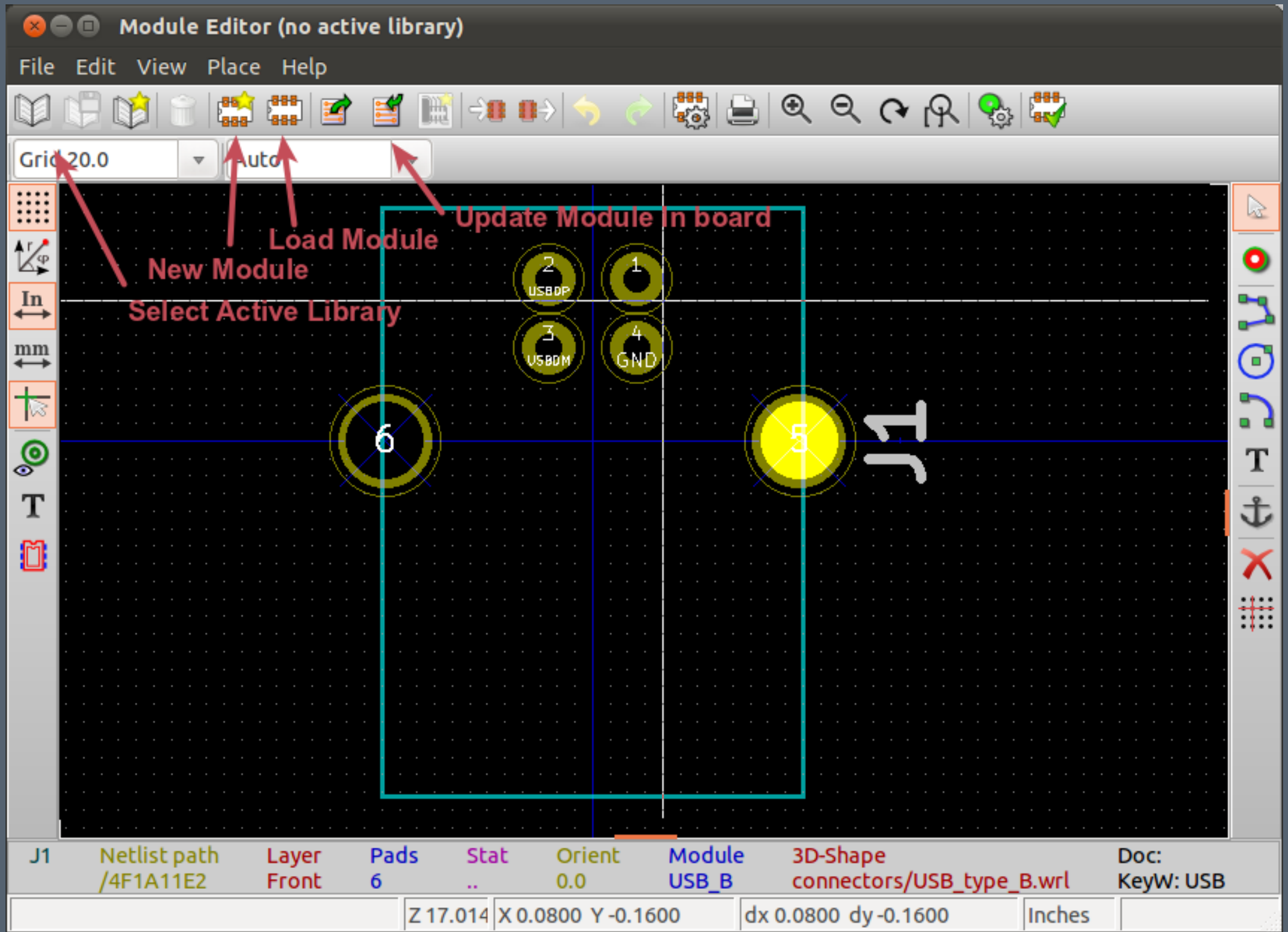
Add Text

Set Relative Origin

Relative Placement

J1	Netlist path	Layer	Pads	Stat	Orient	Module	3D-Shape	Doc:
	/4F1A11E2	Front	6	..	0.0	USB_B	connectors/USB_type_B.wrl	KeyW: USB

Z 17.014 | X 0.0800 Y -0.1600 | dx 0.0800 dy -0.1600 | Inches


Module Editor (no active library)
File Edit View Place Help
Grid 20.0
Auto
Update Module In board
Load Module
New Module
Select Active Library
2
USBDP
1
3
USBDM
4
GND
6
5
J1
J1 Netlist path /4F1A11E2
Layer Front
Pads 6
Stat ..
Orient 0.0
Module USB_B
3D-Shape connectors/USB_type_B.wrl
Doc:
KeyW: USB
Z 17.014
X 0.0800 Y -0.1600
dx 0.0800 dy -0.1600
Inches

Pad Properties

Pad Num : 5

Pad Net Name :

Pad Geometry:

Pad pos X	0.2362	inches
Pad pos Y	0.0000	inches
Pad drill X	0.0906	inches
Pad drill Y	0.0906	inches
Shape size X	0.1063	inches
Shape size Y	0.1063	inches
Shape offset X	0.0000	inches
Shape offset Y	0.0000	inches
Shape delta dim	0.0000	inches
Trap. direction	> ^	Rot 0
Length die	0.0000	inches

Pad Shape:
- (•) Circle
- ( ) Oval
- ( ) Rect
- ( ) Trapezoidal

Drill Shape:
- (•) Circle
- ( ) Oval

Pad Orient:
- (•) 0
- ( ) 90
- ( ) -90
- ( ) 180
- ( ) Custom

Pad Orient (0.1 deg): 0

Footprint orientation
Rotation: 0.0
Board side: Front side

Clearances:
Set these values to 0
to use Parent footprint or global values

Net pad clearance	0.0000	inches
Solder mask clearance:	0.0000	inches
Solder paste clearance:	-0.0000	inches
Solder mask ratio clearance:	-0.0	%

Pad Type:
- (•) Standard
- ( ) SMD
- ( ) Conn
- ( ) NPTH, Mechanical

Layers:

Copper Layers:
- ( ) Front
- ( ) Back
- (•) All Copper Layers
- ( ) No Copper Layers

Technical Layers:
- [ ] Adhes_Front
- [ ] Adhes_Back
- [ ] SoldP_Front
- [ ] SoldP_Back
- [x] SilkS_Front
- [ ] SilkS_Back
- [x] Mask_Front
- [x] Mask_Back
- [ ] Drawings
- [ ] Eco1
- [ ] Eco2

Cancel OK

Done with PCBNew!

Additional Utilities

- KiCad Quick Lib Gen
  - http://kicad.rohrbacher.net/quicklib.php
- FreeRouter
  - http://www.freerouting.net/
- GerbV
  - http://gerbv.sourceforge.net/

END OF LINE